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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,298	04/12/2004	Liping Ren	IR-2390 (2-3	4746

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EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,298	REN, LIPING	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,11,13 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,11,13 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: IR-2390 (2-3965)
Filing Date: 4/12/2004
Claimed Priority Date: 4/11/2003 (Provisional 60/462,562)
Applicant(s): Ren
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 1/22/2007.

Acknowledgment

1. The amendment filed on 1/22/2007, responding to the Office action mailed on 10/18/2006, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-7, 9, 11, 13, and 20-23.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the second portion **33** of the first field plate electrically connected to the second portion **39** of the second field plate by an electrical connector **50** as described in par.0023/ll.6-8 of the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

2. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being

amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

3. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 11, 13, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishima (US6740952) in view of Rumennik (US6639277), Van Zant, Ghandhi, Noda (US6617652), and Ranjan (US5801431).

4. Regarding claim 1, Fujishima shows (see, *e.g.*, figs. 15 and 19) most aspects of the instant invention including a semiconductor device comprising:

- ✓ A semiconductor substrate **1** of a first conductivity type

- ✓ A semiconductor layer of a second conductivity type formed over the substrate **1**
- ✓ A body region **2** of the first conductivity formed in the semiconductor layer
- ✓ An invertible channel in the body region **2**
- ✓ A source region **3** of the second conductivity type formed in the body region **2** and adjacent to the channel
- ✓ A gate structure formed over the channel region including:
  - a gate electrode **9**
  - a gate insulation layer **7** spacing the gate electrode **9** from the channel
- ✓ A drain region **6** formed in the semiconductor layer
- ✓ A drift region **5** in the semiconductor layer spacing the body region **2** from the drain region **6**
- ✓ A resurf region **20** of the first conductivity formed in the semiconductor layer of the second conductivity type, said resurf region **20** being formed over at least a portion of the drift region **5** between the body region and the drain region
- ✓ A field plate structure disposed over the drift region **5** including:
  - a first insulation layer **8** of a first thickness extending from the gate insulation layer
  - a second insulation layer **10** of a second thickness formed over the first insulation layer **8**
  - a third insulation layer **25** of a third thickness

- a first plate **9** disposed over the first insulation layer **8**
- a second plate **FP1** disposed over the second insulation layer **8**
- a third plate **FP2** spaced from the second plate **FP1** by the third insulation layer **25**

Wherein:

- ✓ the first plate **9** includes a first portion extending from the gate electrode (see, *e.g.*, fig. 19)
- ✓ the second plate **FP1** includes (see, *e.g.*, fig. 19):
  - a first portion
  - a second portion
  - a second gap separating the portions
- ✓ the third plate **FP2** includes (see, *e.g.*, fig. 19):
  - a first portion
  - a second portion
  - a third gap **Wg** separating the portions
- ✓ the second gap is wider than the third gap **Wg** (see, *e.g.*, fig. 19)

Fujishima, however, fails to show the first plate including a second portion spaced from the first portion of the first plate by a first gap wider than the second gap. Rumennik (see, *e.g.*, figs. 1 and 2), on the other hand, shows a first plate similar to Fujishima including a first portion **12** spaced from a second portion **26** by a gap wider than the gap separating the portions **10,11** of a second plate above the first plate. He

further teaches that the second portion **26** would function to increase the breakdown voltage of Fujishima (see, *e.g.,* Rumennik/col.4/ll.45).

It would have been obvious at the time of the invention to one of ordinary skill in the art to include the second portion suggested by Rumennik in the first plate of Fujishima to reduce the field concentration at the boundary between the drain region and the drift region.

Fujishima also fails to show the semiconductor layer being epitaxially formed and extending below the body region. Rumennik, on the other hand, shows the semiconductor layer being epitaxially formed (see, *e.g.*, col.7/ll.21) and extending below the body region (see, *e.g.*, fig.5 and fig.6). Van Zant (see, *e.g.*, pp.382), on the other hand, teaches that epitaxially forming Fujishima's semiconductor layer would allow accurate control of the doping concentrations of the layer. Ghandhi (see, *e.g.*, pp.258) teaches that epitaxially forming Fujishima's semiconductor layer on the substrate would eliminate the problems of compatibility or mismatch between the layer and the substrate.

It would have been obvious at the time of the invention to one of ordinary skill in the art to epitaxially form Fujishima's semiconductor layer, as suggested by Van Zant and Ghandhi, to eliminate compatibility problems between the layer and the substrate and to accurately control the doping concentrations of the layer.

Fujishima fails to show the first and second portions of the second field plate, and the first and second portions of the third field plate being circular and disposed around the drain region. Noda, on the other hand, teaches (see, *e.g.*, fig. 1) that annular

circular plates formed concentrically around the drain diffusion region of Fujishima would improve the breakdown properties of the device (see, *e.g.*, Noda/col.14/ll.20-22 and col.9/ll.38). Ranjan elaborates by teaching that the series of plates in Noda reduce the tendency to concentrate high electric fields near the surface of the device thereby improving its breakdown voltage (see, *e.g.*, Ranjan/col.5/ll.52-56).

It would have been obvious at the time of the invention to one of ordinary skill in the art to form the first and second portions of the second and third plates of Fujishima/Rumennik as annular circular portions disposed around the drain region, as suggested by Noda and Ranjan, to improve the breakdown voltage properties of the device.

5. Regarding claims 2, 4, and 6, Fujishima shows the first **8**, second **10** and third **25** insulation layers comprising an oxide (see, *e.g.*, fig. 19)

6. Regarding claim 3, Fujishima shows the first thickness is 0.6 microns (see, *e.g.*, col.36/ll.20) but fails to specify the claimed thickness of 0.4 microns. However, differences in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Fujishima also teaches that the first thickness, as well as the other thickness of the different insulation layers, affects the performance and the area of the device (see, *e.g.*, col.37/ll.15-29, col.8/ll.36-40, and col.39/ll.17-31). Therefore, it is necessary to

ensure that the insulation layers are of an appropriate thickness (see, e.g., Fujishima/col.35/ll.60-62). The specific claimed first thickness, *i.e.*, 0.4 microns, absent any criticality, is only considered to be the "optimum" thickness disclosed by Fujishima that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired device performance, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the first thickness provides for a stable performance of the device, as already suggested by Fujishima.

Since the applicant has not established the criticality (see next paragraph) of the claimed thickness of 0.4 microns, it would have been obvious to one of ordinary skill in the art to use these values in the device of Fujishima.

CRITICALITY

7. The specification contains no disclosure of either the critical nature of the claimed thickness or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. Regarding claim 5, Fujishima shows the second thickness is 1.3 microns (see, *e.g.*, col.39/ll.5).

9. Regarding claim 7, Fujishima shows the third thickness is 2.5 microns (see, *e.g.*, col.39/ll.7) instead of the claimed thickness of 1.4 microns. See also the comments stated above in paragraphs 6 and 7 with respect to the differences between the claimed thickness and that of the prior art, which are considered repeated here.

10. Regarding claim 9, Fujishima shows the first field plate **9** comprising gate electrode material (see, *e.g.*, col.39/ll.9-10). Van Zant (see, *e.g.*, pp. 511), on the other hand, teaches that doped polysilicon is the standard gate electrode material for Fujishima's device.

11. Regarding claim 11, Fujishima shows that the gap between the portions of the second field plate **FP1** is 45 microns (see, *e.g.*, col.37/ll.29-34 and col.39/ll.13-16).

12. Regarding claim 13, Fujishima shows the third field plate **FP2** comprising a first portion and a second portion (see, *e.g.*, fig. 19), wherein a gap of 25 microns separates the portions (see, *e.g.*, col.37/ll.32).

13. Regarding claim 20, Fujishima shows the first portion of the first plate **9** terminating below the first portion of the second plate **FP1** (see, *e.g.*, fig. 19).

14. Regarding claim 21, Fujishima shows the second portion of the second field plate **FP1** is electrically connected to the drain region **6** and to the second portion of the third plate **FP2** (see, *e.g.*, fig. 19).

15. Regarding claim 22, Fujishima shows the first portion of the second plate **FP1** is electrically connected to the first plate **9** (see, *e.g.*, fig. 19).

16. Regarding claim 23, Fujishima shows the first portion of the third plate **FP2** is electrically connected to the source region **3** (see, *e.g.*, fig. 19).

Response to Arguments

17. The applicant argues:

> Claim 1 calls for the epitaxially formed semiconductor layer to extend below the body region. Fujishima, however, only shows the semiconductor layer **5** and the body region **2** adjacent along a vertical wall. The semiconductor layer **5** does not extend below the body region **2**.

18. The examiner responds:

Rumennik clearly shows the above features of the claimed invention. See, *e.g.*, figs. 5 and 6, where Rumennik shows the epitaxially formed semiconductor layer **106** extending below the body region **110/111**.

19. The applicant argues:

Claim 1 calls for the first and second portion of the second and third field plates to be circular and disposed around the drain region. No reference has been shown that teaches or suggests such features.

20. The examiner responds:

Noda and Ranjan clearly show these features of the claimed invention. See, *e.g.*, fig. 1, where Noda teaches that annular circular plates formed concentrically around the drain diffusion region of Fujishima would improve the breakdown properties of the device (see, *e.g.*, Noda/col.14/ll.20-22 and col.9/ll.38). Ranjan elaborates by teaching that the series of plates in Noda reduce the tendency to concentrate high electric fields near the surface of the device thereby improving its breakdown voltage (see, *e.g.*, Ranjan/col.5/ll.52-56).

21. The applicant argues:

No single embodiment cited by the examiner discloses the field plate structure recited in claim 1.

22. The examiner responds:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Fujishima shows most aspects of the instant invention as set forth above in paragraph 4 of the present Office action. Fujishima, however, fails

to show the first plate including a second portion spaced from the first portion of the first plate by a first gap wider than the second gap. Rumennik (see, *e.g.*, figs. 1 and 2), on the other hand, shows a first plate similar to Fujishima including a first portion **12** spaced from a second portion **26** by a gap wider than the gap separating portions **10,11** of a second plate above the first plate. He further teaches that the second portion **26** would function to increase the breakdown voltage of Fujishima (see, *e.g.*, Rumennik/col.4/ll.45).

23. The applicant argues:

> Rumennik discloses a structure significantly different from the embodiments of Fujishima. Rumennik discloses a source electrode **10** and a drain electrode **11** located near the top surface of the die. Fujishima by contrast discloses a source electrode **11** and a drain electrode layer **12** located in the middle of the embodiment of the die shown in figure 19. Thus, to arrive at the proposed combination to make the rejection, it is necessary for the examiner to seize upon arbitrarily selected features of Rumennik and then insert them into the middle of the die shown in Fujishima at a location selected by the examiner, and further, to change functions of the inserted embodiments. In addition, it would be necessary to seize the p-type top layer **20** of the third embodiment of Fujishima shown in figure 15, and insert this into the seventh embodiment of Fujishima shown in figure 19 just below the features taken from Rumennik.

24. The examiner responds:

In contrast to applicant's assertions, Rumennik discloses a structure significantly similar to the embodiments of Fujishima. Both show high-voltage lateral MISFETs having a polysilicon gate and a gate-insulating layer on a p-type substrate (see, *e.g.*, Rumennik: fig.2, and Fujishima: figs. 15 and 19). The gate, gate-insulating layer, and substrate form an insulated gate region in the devices of both Rumennik and Fujishima. Additionally, source and drain electrodes as well as a field plate structures are formed over the insulated gate regions of both devices.

On the other hand, the seventh embodiment of Fujishima (see, *e.g.*, fig. 19) has exactly all the features of the third embodiment of Fujishima (see, *e.g.*, fig. 15) but the p-

type top layer **20**. In any event, Fujishima clearly teaches that there is an advantage to incorporating the p-type top layer **20** of the 3rd embodiment into the 7th embodiment in that, as well as being able to provide the n-type drift region **5** with a high concentration, it is possible to maintain the withstand voltage, and a reduction in the ON resistance is also effected (see, *e.g.*, col.37/ll.50-60).

25. The applicant argues:

> The teachings cited by the examiner of reducing the field concentration at the boundary between the drain region and the drift region is too general to provide the motivation necessary for arriving at the proposed combination, involving features of two separate embodiments of Fujishima and additional features selected from Rumennik.

26. The examiner responds:

The teachings of Rumennik are clear and precise. Rumennik (see, *e.g.*, figs. 1 and 2) shows a first plate similar to Fujishima including a first portion **12** spaced from a second portion **26** by a gap wider than the gap separating portions **10,11** of a second plate above the first plate. He specifically teaches that the second portion **26** would function to increase the breakdown voltage of Fujishima (see, *e.g.*, Rumennik/col.4/ll.45).

27. The applicant argues:

> The problems recognized by the applicants and solved by the claimed invention, such as the issue of reducing high electric field gradients at the surface of a semiconductor die, are not disclosed or suggested by the cited references.

28. The examiner responds:

The fact that the applicant has recognized another advantage that would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious as set forth in

paragraphs 4-27 above. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

33. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

34. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/335-343,409,487,488,491-493,659	2/28/2007
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	2/28/2007

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